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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,665	05/21/2004	Hsin-Wo Fang	NAUP0592USA	3664

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
04/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,665	FANG ET AL.	
	Examiner	Art Unit	
	HELEN ROSSOSHEK	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-10 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/709,665 filed 05/21/2004 and amendment filed 01/29/2008.

2. Claims 1-3, 5-10 and 12-15 remain pending in the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/29/2008 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5, 7-10, 12, 14, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Bansal (US Patent 5,858,817).

With respect to claim 1 Bansal teaches a method for implementing circuit layouts in a chip (within a method for design and fabricating integrated circuit (ASIC) (col. 1, ll.7-10)), comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip, where each sub-circuit cell comprising at least two types of sub-circuit blocks

(within placing plurality of multi-function logic cells 18 and multi-function logic cells 10 in different positions of the chip as shown on the Fig. 8 (col. 5, ll.37-37-38), wherein, for example, the multi-function logic cells 10 have similar layout, comprising the same logic elements as sub-circuit blocks (col. 3, ll.21-25)); and

when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells, wherein each layout in the connection layer corresponding to each sub-circuit cell creates a connection between some of the sub-circuit blocks within each corresponding sub-circuit cell be selectively connecting the sub-circuit blocks within each corresponding sub-circuit cell, and short-circuits the rest of the sub-circuit blocks within each sub-circuit cell not connected together to DC bias voltages of the chip, so that the sub-circuit cells in different positions implement different circuit functions (within input and output buffer cells 18 shown on the Fig. 8 are placed in different positions on the periphery of a chip 50, wherein any cell 18 can perform different function (col. 5, ll.37-41), wherein implementation of the different functions is achieved by completing the cell internal interconnections with the single masking step which completes the connections within the multi-function logic cell 18 or 10 (col. 5, ll.42-45), and wherein the internal interconnections within cells 18 are completed in a manner similar to that used to complete the internal interconnections within cells 10 (col. 5, ll.46-49), and wherein complete layout of the cells 18 is predefined up to third metallization level (the same for all cells 18) (col. 2, ll.12-14; ll.3-12) and the function of the cell 18 is established within

third metal level by personalizing the third metal level (i.e. selectively connecting components of the cell 18 (col. 2, ll.26-31), and wherein outputs of unused sub-circuit blocks (not connected together) are tied to "V"/DC bias voltages as shown on Fig. 6 for cell 10 (col. 4, ll.64-66; col. 3, ll.40-44), which will be similar for cells 18, since, as was mentioned above, internal interconnections within cells 18 are completed in a manner similar to that used to complete the internal interconnections within cells 10 (col. 5, ll.46-49)).

With respect to claim 9 Bansal teaches a method for implementing circuit layouts in a chip (within a method for design and fabricating integrated circuit (ASIC) (col. 1, ll.7-10)), comprising:

a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout, each sub-circuit cell comprising at least two types of sub-circuit blocks (within placing plurality of multi-function logic cells 18 and multi-function logic cells 10 laid out within plurality of layers in different positions of the chip as shown on the Fig. 8 (col. 5, ll.37-37-38; col. 2, ll.1-2), wherein, for example, the multi-function logic cells 10 have similar layout, comprising the same logic elements as sub-circuit blocks (col. 3, ll.21-25)); and

at least a connection layer comprising different layouts corresponding to the different positions of the layout layers, wherein each layout of the connection layer creates a connection between the sub-circuit blocks within each corresponding sub-circuit cell so that the sub-circuit cells in different positions implement different circuit

functions (within input and output buffer cells 18 shown on the Fig. 18 are placed in different positions on the periphery of a chip 50, wherein any cell 18 can perform different function (col. 5, ll.37-41), wherein implementation of the different functions is achieved by completing the cell internal interconnections with the single masking step which completes the connections within the multi-function logic cell 18 or 10 (col. 5, ll.42-45), and wherein the internal interconnections within cells 18 are completed in a manner similar to that used to complete the internal interconnections within cells 10 (col. 5, ll.46-49), and wherein complete layout of the cells 18 is predefined up to third metallization level (the same for all cells 18) (col. 2, ll.12-14; ll.3-12) and the function of the cell 18 is established within third metal level by personalizing the third metal level (i.e. selectively connecting components of the cell 18 (col. 2, ll.26-31)).

With respect to claim 9 Bansal teaches limitations similar to the claim 1 including a chip (within a chip schematically shown on the Fig. 8 (col. 5, ll.37-50)).

With respect to claims 2-5, 7, 8, 10-12, 14 and 15 Bansal teaches:

Claims 2, 10: wherein the connection layer is a metal layer (col. 3, ll.36-38);

Claim 3: the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer (col. 3, ll.29-33; 36-39);

Claims 5, 12: wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions (col. 5, ll.37-43);

Claims 7, 14: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates (col. 5, ll.39-41);

Claims 8, 15: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents (col. 5, ll.39-41).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bansal as applied to claims 1 and 9 above, and further in view of Maeda (US Patent 6,052,014).

With respect to claims 6 and 13 Bansal teaches the limitation from which claims depend including multi-function logic sells 10 and 18 being placed at any position in the layout of the integrate circuit including in the input/output area implementing multiple functions. However Bansal lacks specifics regarding implementing a Schmidt trigger function by I/O circuit. Maeda teaches:

Claims 6, 13: wherein the sub-circuit cells in different positions are for implementing I/O circuit with a Schmidt trigger function (col. 1, ll.59-63). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Maeda to teach the specifics subject matter Bansal does not teach, because there is an ability of transferring signals of different voltage levels between the internal circuit and the circuits constructing the input/output circuit and performing slew rate control (abstract of Maeda).

Remarks

8. In remarks Applicant argues in substance:

a) "Bansal ... fails to teach or suggest short-circuiting the sub-circuit blocks to DC bias voltages of the chip".

9. Examiner respectfully disagrees for the following reasons:

With respect to a) Bansal teaches outputs of unused sub-circuit blocks (not connected together) are tied to "V"/DC bias voltages as shown on Fig. 6 for cell 10 (col. 4, ll.64-66; col. 3, ll.40-44), which will be similar for I/O cells 18, since internal interconnections within cells 18 are completed in a manner similar to that used to complete the internal interconnections within cells 10 (col. 5, ll.46-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELEN ROSSOSHEK whose telephone number is (571)272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
03/27/2008

/Helen Rossoshek/
Examiner
Art Unit 2825